Revision history

Revision	Release data	Description

GENERAL DESCRIPTION

The HM6601Q is a fast charging protocol controller for HiSilicon Fast Charging Protocol (FCP) and QC 2.0/3.0 USB interface. The HM6601Q monitors USB D+/D− data line and automatically adjusts the output voltage depending on different powered device (PD). The charging time of PD is therefore optimized by the HM6601Q

HM6601Q can support not only USB BC compliant devices, but also Apple / Samsung / HUAWEI devices and automatically detects whether a connected powered device is QC 2.0/3.0 or FCP capable before enabling output voltage adjustment. If a PD is not compliant with QC 2.0/3.0 and FCP, the HM6601Q will disable the adjustment of output voltage and keep the default 5V output voltage for safe operation.

The HM6601Q is available in a space-saving SOT23-6 package.

FEATURES

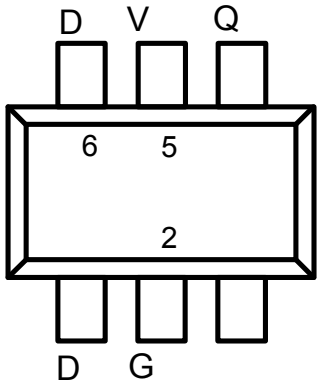
- Supports HiSilicon Fast Charging Protocol (FCP)
- Supports Qualcomm® Quick ChargeTM 2.0/3.0

  Class A : 3.6V up to 12V Output Voltage
- Automatically Selects FCP and QC2.0/3.0 Protocols
- Supports USB DCP Shorting D+ Line to D− Line per USB Battery Charging Specification, Revision 1.2
- Complies with Chinese Telecommunication Industry Standard YD/T 1591-2009
- Supports USB DCP Applying 2.7V on D+ Line and 2.7V on D− Line

APPLICTIONS

- Wall-Adapter, Smart Phones, Tablets, Notebooks
- Mobile / Tablet Power Bank
- Car Charger
- USB Power Output Ports

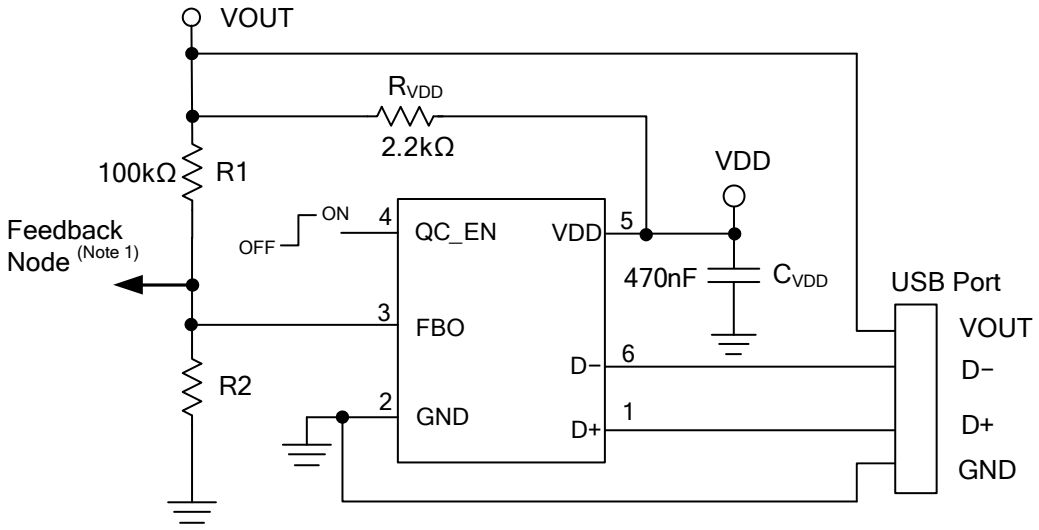
PIN ASSIGNMENTS



FUNCTIONAL PIN DESCRIPTION

Pin Name	Pin No.	Pin Function
D+	1	USB D+ data line. Recommended this pin connect without resistors(open) or with a resistor higher than 1MΩ connect to GND.
GND	2	Ground pin.
FBO	3	Feedback output pin. Current sink/source FB node.
QC_EN	4	QC_enable: QC2.0/3.0 and FCP function are enabled by either logic high or high-Z. Contrarily, QC2.0/3.0 and FCP function are disabled by logic low.
VDD	5	Power supply input pin.
D−	6	USB D− data line.

TYPICAL APPLICATION CIRCUIT

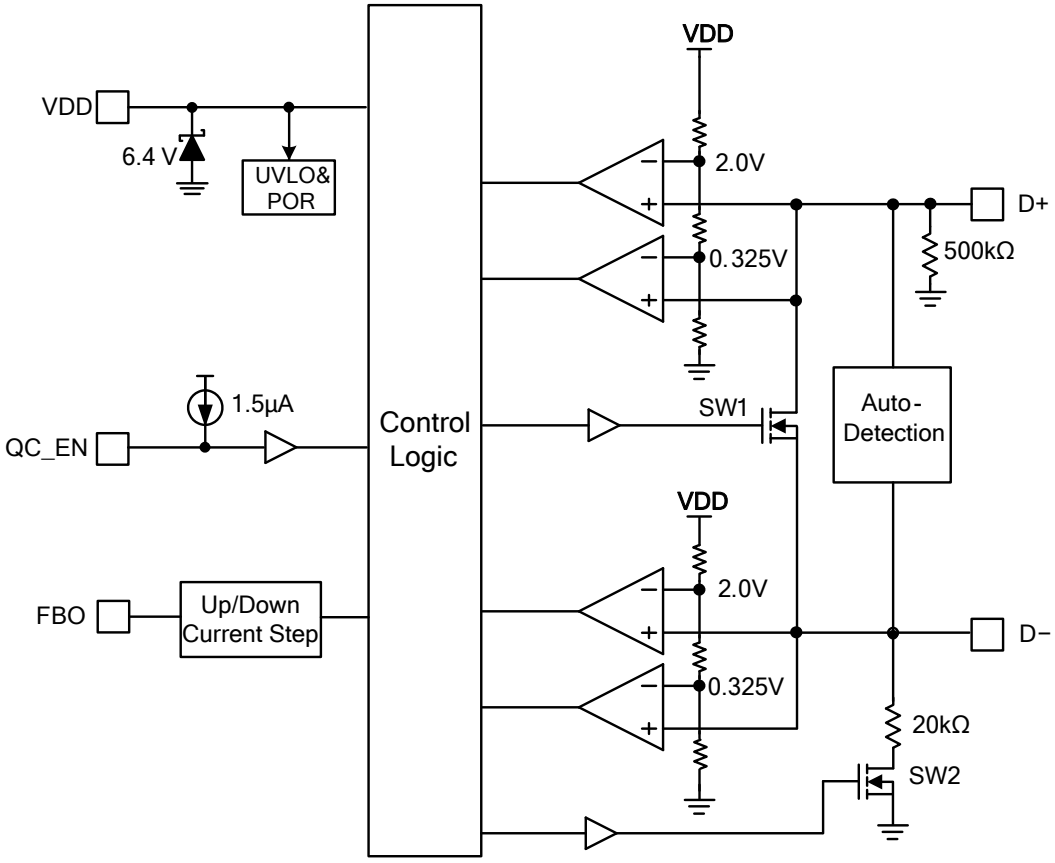


Note 1: The recommended voltage of feedback node ranges between 0.4V and 1.5V

OUTPUT VOLTAGE LOOKUP TABLE (QC 2.0/3.0)

D+	D-	Output Voltage
0.6V	0.6V	12V
3.3V	0.6V	9V
0.6V	3.3V	Continuous mode
0.6V	High-Z	5V (Default)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 2)

- Input Supply Voltage VDD ---------- -0.3V to +7V
- D+,D−Pins Voltage ---------- -0.3V to +14V
- All Other Pins Voltage ---------- -0.3V to +7V
- Maximum Junction Temperature (T_J)---------- +150℃
- Storage Temperature (T_S)---------- -65℃ to +150℃
- Lead Temperature (Soldering, 10sec.) ---------- +260℃

● Package Thermal Resistance, (θ_{JA}) (Note 3)

SOT-23-6---------- 250°C/W

● Package Thermal Resistance, (θ_{JC})

SOT-23-6---------- 110°C/W

Note 2: Stresses beyond this listed under “Absolute Maximum Ratings" may cause permanent damage to the device.
Note 3: θ_{JA} is measured at 25°C ambient with the component mounted on a high effective thermal conductivity test board of JEDEC-51-7.

RECOMMENDED OPERATING CONDITIONS

● Input Supply Voltage (VDD)---------- +3.2V to +6.8V

● Operation Temperature Range (T_{OPR}) ---------- -40°C to +85°C

ELECTRICAL CHARACTERISTICS

(VDD=5V, T_A=25°C and the recommended supply voltage range, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Section						
VDD Input Voltage Range	V_{DD}		3.2		6.8	V
Input UVLO Threshold	$V_{UVLO(VTH)}$	V_{DD} Falling	2.5		2.9	V
VDD Supply Current		V_{DD} =5V, Measure V_{DD}		180		μA
VDD Shunt Voltage	$V_{DD(SHUNT)}$	I_{VDD} = 3mA	5.9	6.4	6.8	V
High Voltage Dedicated Charging Port (HVDCP)						
Data Detect Voltage	$V_{DAT(REF)}$		0.25	0.325	0.4	V
Output Voltage Selection	V_{SEL_REF}		1.8	2.0	2.2	V
D+ High Glitch Filter Time	$T_{GLITCH(BC)-D+\_H}$		1000	1250	1500	ms
D− Low Glitch Filter Time	$T_{GLITCH(BC)-D-\_L}$			1		ms
Output Voltage Glitch Filter Time	$T_{GLITCH(V)CHANGE}$		20	40	60	ms
D− Pull-Down Resistance	$R_{D-(DWN)}$			20		kΩ
Continuous Mode Glitch Filter Time (Note 4)	$T_{GLITCH-CONT-CHANGE}$		100		200	μs
D+ Leakage Resistance	$R_{DAT-LKG}$	V_{DD} =3.2-6.4V, V_{D+}=0.6-3.6V Switch SW1=Off	300	500	800	kΩ
Switch SW1 On-Resistance	$R_{DS\_ON\_N1}$	V_{DD} =5V, SW1= 200μA			40	Ω

Up/Down Current Step	I_{UP}, I_{DOWN}	I_{UP} = 40μA (9V), 70μA (12V), I_{DOWN} = 14μA (3.6V)		2		μA
Feedback Output Voltage	V_{FBO}		0.4		1.5	V
DCP Charging Mode						
$D+_{\_0.48V}$/$D-_{\_0.48V}$ Line Output Voltage			0.44	0.48	0.52	V
$D+_{\_0.48V}$/$D-_{\_0.48V}$ Line Output Impedance				900		kΩ
Apple Mode						
$D+_{\_2.7V}$/$D-_{\_2.7V}$ Line Output Voltage			2.57	2.7	2.84	V
$D+_{\_2.7V}$/$D-_{\_2.7V}$ Line Output Impedance				33.6		kΩ
D− SECTION (FCP)						
D− FCP Tx Valid Output High	V_{TX-VOH}		2.55		3.6	V
D− FCP Tx Valid Output Low	V_{TX-VOL}				0.3	V
D− FCP Rx Valid Output High	V_{RX-VIH}		1.4		3.6	V
D− FCP Rx Valid Output Low	V_{RX-VIL}				1.0	V
D− Output Pull-Low Resistance (FCP) (Note 4)	R_{PD}		400	500	600	Ω
Unit Interval For FCP PHY Communication	UI	f_{CLK} = 125kHz	144	160	180	μs
Others						
QC_EN High-Level Input Voltage	V_{IH}		1.2			V
QC_EN Low-Level Input Voltage	V_{IL}				0.4	V

APPLICATION INFORMATION

FUNCTION DESCRIPTION

The HM6601Q integrates both USB high voltage dedicated charging port interface IC for QC 2.0 and QC3.0 class A and HiSilicon FCP specification.

The HM6601Q can fast charge most of the handhold devices. It could be treated as the original charging adapter.

The HM6601Q supports BC1.2, Samsung and HUAWEI devices. It also supports output voltage

range of QC 3.0 Class A (3.6V to 12V) or QC 2.0 Class A (5V, 9V, 12V).

QUICK CHARGE 2.0/3.0 INTERFACE

When the HM6601Q is powered on, D+ and D− pin are applied to 2.7V for Apple device. If handhold device has the function of QC 2.0/3.0, D+ pin will be forced between 0.325V and 2V. In the meanwhile, D+ pin will short to D− pin through the switch SW1 for entering BC 1.2. If D+ is continuously applied to the voltage between 0.325V and 2V for 1.25 seconds, the HM6601Q will enter QC 2.0/3.0 or FCP operation mode.

When the voltage of D+ pin and D− pin simultaneously satisfy these two inequalities VDAT(REF)< D+ <VSEL_REF and D− > VSEL_REF, the HM6601Q would enter continuous mode.

In the continuous mode, each voltage pulse on D+ pin generated by powered device is between 1V and 3V. In the meanwhile, the high level of pulse should be keep at least 200us. If the specified conditions are satisfied, the FBO pin will sink 2uA per pulse. The maximum sink current is 70uA for output voltage 12V.

In the continuous mode, each voltage pulse on D− pin generated by powered device is between 3V and 1V. At the same time, the low level of pulse should be keep at least 200us. If the specified conditions are satisfied, the FBO pin will source 2uA per pulse. The maximum source current is 14uA for output voltage 3.6V.

If the powered device doesn't support QC 2.0, the HM6601Q will remain default output voltage 5V for safe operation. On the other hand, when USB cable is removed, the voltage of D+ pin is therefore lower than VDAT(REF) and the output default voltage 5V is also applied.

SHUNT REGULATOR

The VDD of HM6601Q is supplied by the wide output voltage through the external resistor RVDD. The internal Zener-Diode is utilized to clamp the VDD at 6.4V. The recommended value of RVDD and CVDD are 2.2kΩ and 470nF, respectively.

QC_EN FUNCTION

QC 2.0/3.0 and FCP function are disabled by connecting the QC_EN pin to ground. On the contrary, QC 2.0/3.0 and FCP function could be enabled by connecting QC_EN pin to VDD or high. Additionally, when HM6601Q is already accessed QC 2.0/3.0 or FCP mode, the selected mode can't be changed by setting QC_EN pin.

DATA LINE PROTECTION

When D+/D− pin is touched by the output voltage in abnormal situation, the D+/D− pin of both sink device and source device may be damaged. In order to protect the D+/D− pin of the devices from damage in abnormal situation, the HM6601Q will return the output voltage to default output voltage 5V when the voltage of D+/D− pin is touched larger than 7.5V.

PACKAGE INFORMATION

SOT23-6